AN INVESTIGATION OF TURN-OFF PERFORMANCE OF PLANAR AND TRENCH GATE IGBTS UNDER SOFT AND HARD SWITCHING

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Abstract: **This paper presents the results of an investigation into the turn-off performance of planar and trench gate IGBTs under conditions of soft and hard switching topologies. Voltage and current waveforms, power losses, electric field distributions, and carrier behaviors inside the chips are studied through simulation and experiment. It is noted that the trench gate IGBT has advantage over the planar gate IGBT for hard switching application. On the other hand, the turn-off loss of the planar gate IGBT under soft switching application is slightly lower than that of the trench gate IGBT.**

Ⅰ. INTRODUCTION

IGBTs (Insulated Gate Bipolar Transistor) are now widely used for hard switching power converters but have not yet reached the same level of popularity in soft switching applications, especially in high power use. Recently, the application of IGBTs to soft switching equipment has increased based on the advantages that soft switching technology has in addressing such application problems as power dissipation, noise, operating frequency limit, and stresses impressed on the motors and IGBTs themselves.

The analyses of dynamic operation for a conventional planar gate IGBT and a newly developed trench gate IGBT under soft and hard switching conditions are carried out through both simulation and experimental measurement. The dependencies of dynamic characteristics on such parameters as voltage, current, gate resistance, and temperature are also investigated. Moreover, the electric field, electric potential, and carrier concentration distribution inside the chips under soft and hard switching conditions are analyzed by the aid of simulation. Based on these results, the suitability of IGBTs for soft and hard switching applications is studied.

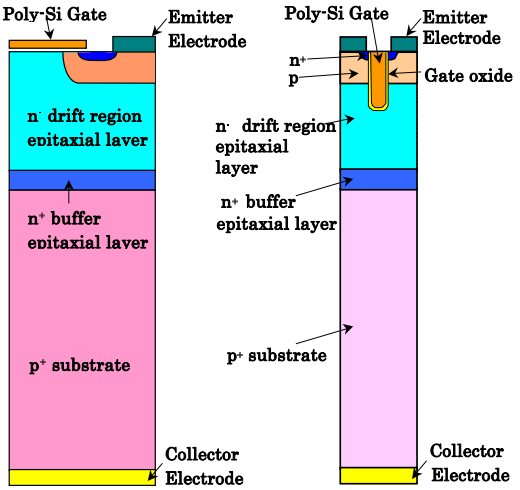
Ⅱ. INVESTIGATION METHOD

A. *Types of IGBTs*

The IGBTs used for simulation analysis and experimental evaluation are Punch Through (PT) type, i.e., buffer layer design, constructed on epitaxial wafers with ratings of 1200V and 50A. The prototype chips are assembled in the latest power module packages with low internal inductance. The specifications and structures are shown in Table 1 and Fig. 1.

Table 1 Types of IGBTs used for analysis

	Type A	Type B
Gate structure	Planar	Trench
On-state voltage at I_C=50A	2.9 V	1.9 V
Current density at I_C=50A	100A/cm^2	140A/cm^2
n+ buffer layer	without local lifetime control	with local lifetime control
Lifetime control over whole wafer	Yes	No
Design rule	3 μm	1μm



(a) Type A (Planar gate) (b) Type B (Trench gate)

Fig. 1 Basic structures of IGBTs used for analysis

The type A IGBT is the typical 3rd generation IGBT with planar gate structure. The lifetime of the whole chip area of type A is controlled by electron beam irradiation. The n+ buffer layer is formed by utilizing proton irradiation which is very effective for improving on-state and switching characteristics and break over voltage without negative trade-offs.

Type B is the newly developed IGBT with the trench gate structure. The trench gate IGBT has such features as very low on-state voltage and on-state loss because it has the gate perpendicular to the silicon surface and a finer gate pattern compared to the standard planar gate IGBT [1], [2], [3]. This type also has an n+ buffer layer and the lifetime in this layer is locally controlled by adjusting annealing time.

B. Simulation and experimental method

The simulation is carried out using the simulation software "MEDICI" under both soft switching and hard switching conditions. Fig. 2(a) illustrates the circuit diagram used for simulation analysis. This circuit is a type of zero voltage switching (ZVS) circuit. The rate of rise of off-state voltage (dv/dt) is set by adjusting the capacitor (C1) and the dv/dt is expressed by the equation:

$$dv/dt = I_C / C1 \qquad (1)$$

The maximum collector voltage (V_{CC}) of the IGBT is set by the avalanche voltage of diode D_{AV}.

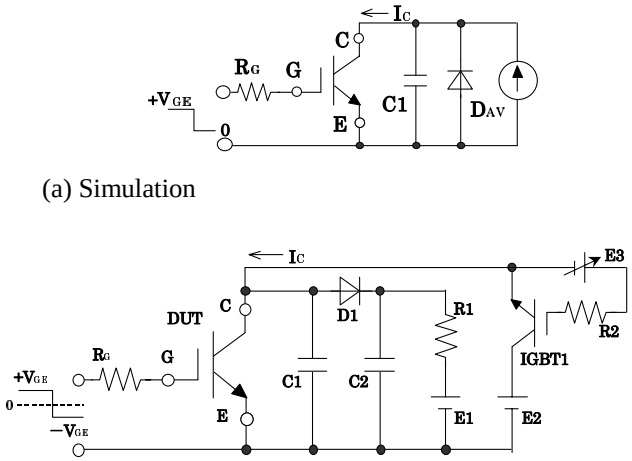
The voltage and current waveforms and switching losses are simulated for both IGBTs and the electric field, potential, and carrier concentration distribution in the IGBT chips are analyzed.

Moreover, experimental measurement and evaluation are performed by utilizing the circuits illustrated in Fig. 2(b). Dv/dt is set by C1 as mentioned above and I_C is set by adjusting the gate voltage E3. The capacitance of C2 is large compared with that of C1 and is charged to the constant voltage, V_{CC}, through R1 by E1. The maximum applied voltage to C1 and the DUT is limited to V_{CC}. The voltage and current waveforms and switching losses are measured and evaluated at varying conditions of collector current, dv/dt, gate resistance, and junction temperature.

Ⅲ. PERFORMANCE ANALYSIS UNDER SOFT AND HARD SWITCHING

A. Current and voltage waveforms

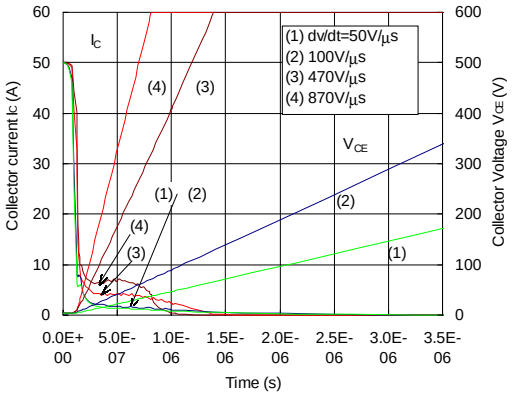
Current and voltage waveforms obtained by simulation are illustrated in Fig. 3. These figures show the waveforms for both types of IGBTs under several dv/dt conditions during turn-off. As seen here, the turn-off operation of type B delays about 0.2μs under soft switching conditions compared with type A. The reason for the delay is that type B has the trench gate structure and its gate capacitance is almost 3 times larger than that of type A.



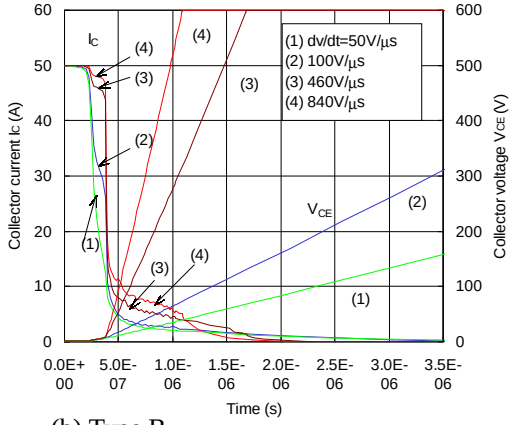
(a) Simulation

(b) Experiment

Fig. 2 Circuit Diagrams used for simulation and experiment



(a) Type A



(b) Type B

Fig.3 Simulated waveforms under soft switching (V_{CC}=600V, I_C=50A, R_G=6.2Ω, Tj=125°C)

The tail current under soft switching condition becomes smaller as dv/dt decreases, but the tail time becomes longer. The tail current of type B is a little higher compared with type A because of its higher current density. The lifetime of type A is controlled over the whole chip area, while that of type B is locally controlled in the n+ buffer layer only. Therefore, the tail time of type A is shorter than that of type B.

The experimentally measured waveforms for both types under hard and soft switching conditions are illustrated in Fig. 4 and Fig. 5. As seen in these figures, under the hard switching condition, the current during the fall time of type B is lower than that of type A. Accordingly, the turn-off loss of type B is lower than that of type A. This demonstrates how effective the local life time control technique is for IGBTs intended for hard switching applications. But under soft switching conditions, the tail current and tail time of type A are a little bit lower than those of type B.

Additionally, the influence of gate resistance on current and voltage waveforms and turn-off loss were investigated experimentally by changing the gate resistance from 3Ω to 20Ω and the following results were obtained. The gate resistance significantly affects the current and voltage waveforms and turn-off loss under hard switching condition, but does not have much influence on them within the range of above mentioned resistances under soft switching condition.

Both the simulated and experimental waveforms closely agree and it is estimated that the slight difference between the waveforms comes from the stray inductance inside the IGBT modules, which is not taken into consideration in the simulation.

B. Turn-off loss

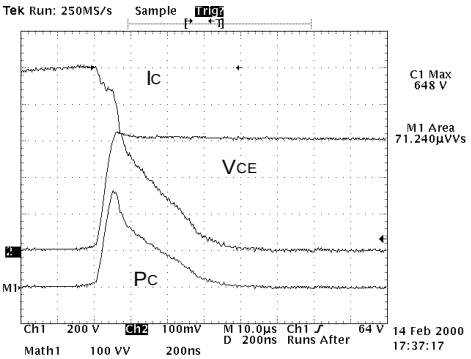
The turn-off losses (E_{off}) calculated from measured switching waveforms for both IGBTs are compared in Fig. 6. The relations between E_{off} and dv/dt are displayed in Fig. 6(a). As shown, the turn-off losses under the soft switching condition, low dv/dt, become very low. For example, the turn-off losses at the condition of 100V/μs are only about 5 to 10 percent of those under the hard switching condition (at dv/dt = 5000V/μs).

The turn-off loss of type B is lower than that of type A under the hard switching condition. On the other hand, the turn-off loss of type A becomes slightly lower than that of type B below 200V/μs.

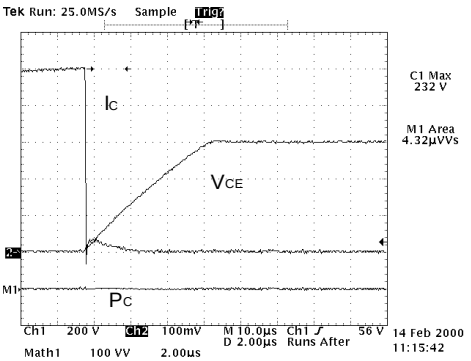
The temperature dependencies on E_{off} for both type A and B are shown in Fig. 6(b). The trend of both characteristics are similar under hard switching condition, but E_{off} of type A becomes much lower as Tj decreases under soft switching conditions. The main reason is that the lifetime of type A becomes shorter at lower temperatures compared with type B.

Fig. 6(c) shows the E_{off} -I_C characteristics for both types. E_{off} of type B is lower than that of type A under the hard switching condition (at dv/dt= 5000V/μs). On the other hand, E_{off} of type B becomes a little higher than that of type A below currents of 75A under the soft switching condition (dv/dt= 100V/μs).

The simulated switching losses agree well with the measured values of the experimental results.

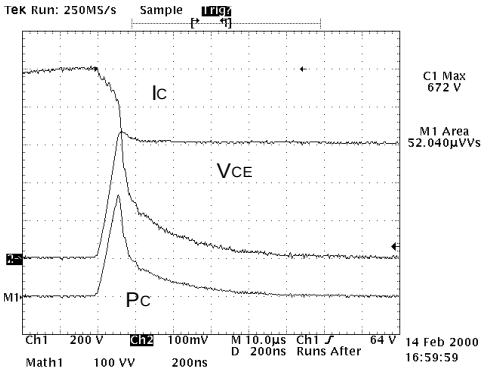


(a) Hard switching
(dv/dt= 5000V/μs, t: 200ns/div.)

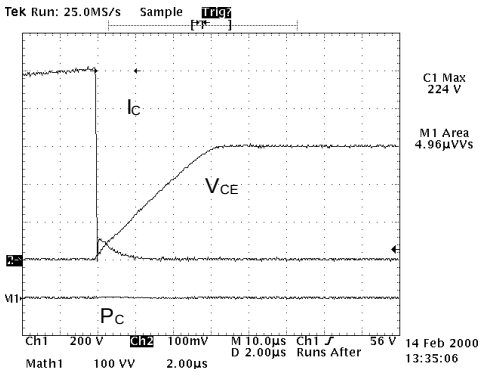


(b) Soft switching
(dv/dt= 100V/μs, t: 2μs/div.)

Fig. 4 Experimentally measured waveforms of type A (The same condition as Fig. 3.)

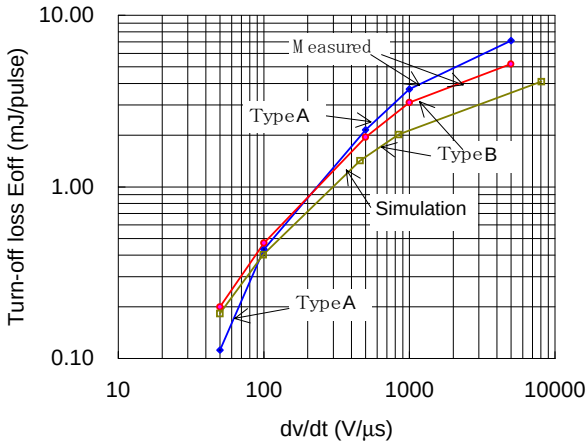


(a) Hard switching
(dv/dt= 5000V/µs, t: 200ns/div.)

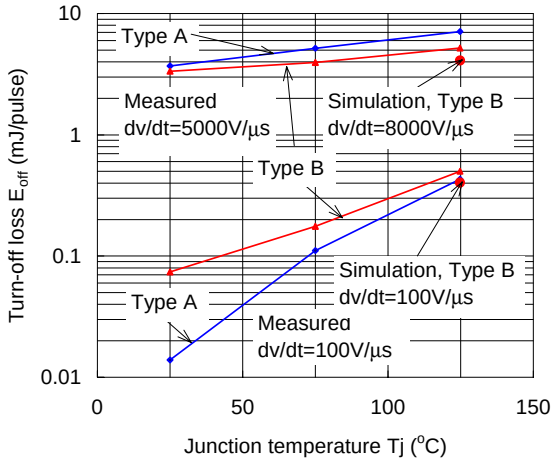


(b) Soft switching
(dv/dt= 100V/µs, t: 2µs/div.)

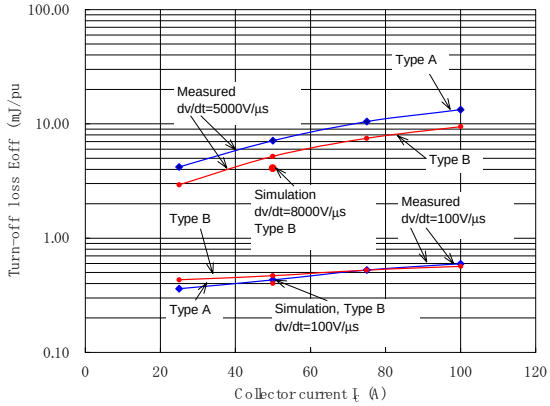
Fig. 5 Experimentally measured waveforms of type B
(The same condition as Fig. 3.)



(a) E_{off} vs. dv/dt



(b) E_{off} vs. Tj



(c) E_{off} vs. I_C

Fig. 6 Dependencies of turn-off loss on dv/dt, collector current, and junction temperature.
(The same condition as Fig. 3.)

C. Analysis inside the chips

The simulated results of electric fields, electric potentials, and the carrier behaviors inside the IGBT chips for type A and type B are displayed in Fig. 7 and Fig. 8 respectively. As seen in these figures, the space charge layer (SCL) spreads slowly because of low dv/dt under the soft switching conditions. This slower expanding speed of the SCL induces longer tail time. For example, the width of the SCL of type A is about 35µm at 0.8µs and 70µm at 3.0µs at the condition of dv/dt=100V/µs as shown in Fig. 7. And, by comparing Fig. 7(b) and Fig. 8(b), it is found that the width of the SCL of type B is narrower compared with that of type A. The underlying reason is that the start of the spreading of the SCL for type B is delayed because of the higher gate capacitance.

Furthermore, it is clear from Fig. 7 and Fig. 8 that only hole current contributes to the tail current and there is no electron current during the tail duration.

Ⅳ. DISCUSSION

It is explained that the reason why the turn-off loss of type B is lower than that of type A under hard switching conditions as shown in Fig. 6 is that type B has an n+ buffer layer with local lifetime control by proton irradiation. Therefore, the lifetime in the n+ buffer layer of type B is shorter than that of type A and the tail current is lower. This technique is very effective for not only improving the break-over voltage and on-state voltage but also lowering the turn-off loss under hard switching operation.

The turn-off loss of type B under soft switching condition is slightly higher than that of type A or close to the same level. The reason is as follows. The lifetime of type A is controlled over whole wafer and type B has the n+ buffer layer with local lifetime control. It seems that while each method strongly affects the tail current under hard switching conditions, there are not large differences between the effects of both methods under low dv/dt conditions and the method of type A is only somewhat more effective under low dv/dt conditions at lower currents.

In considering that the on-state loss of trench IGBT is very low compared with the planar gate IGBT, we can say that the trench gate IGBT (type B) is suitable for soft switching application as well.

Ⅴ. CONCLUSIONS

The switching performance of IGBTs was studied under soft and hard switching conditions. The current and voltage waveforms, switching loss, electric field and potential, and carrier behavior inside the IGBT chips were analyzed at various conditions. It is concluded that the trench gate IGBT with n+ buffer layer and local lifetime control has advantage over the planar gate IGBT under hard switching conditions. Under soft switching conditions, the planar gate IGBT, in which lifetime is controlled over whole chip, has a slight advantage over the trench gate IGBT from the point of turn-off loss. But the trench gate IGBT is also suitable for soft switching application because of lower on-state loss.

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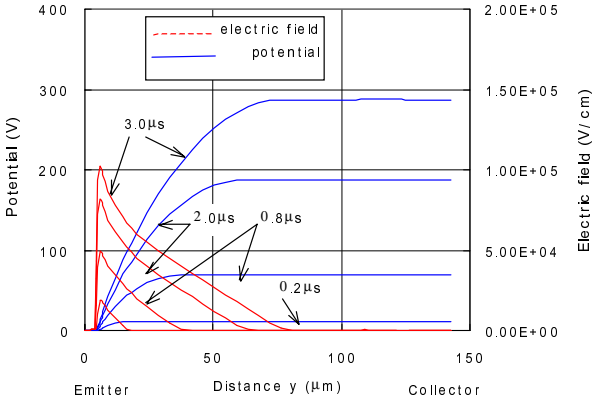
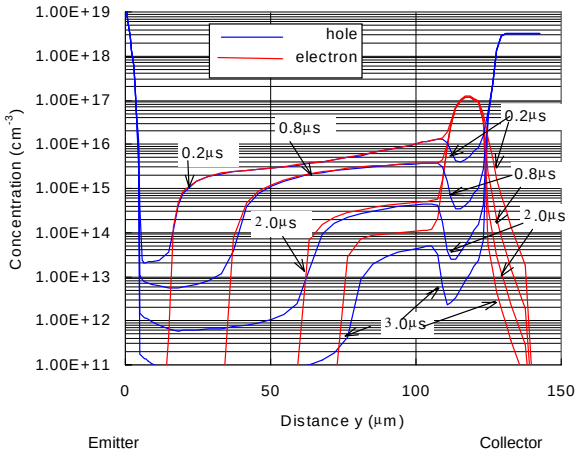
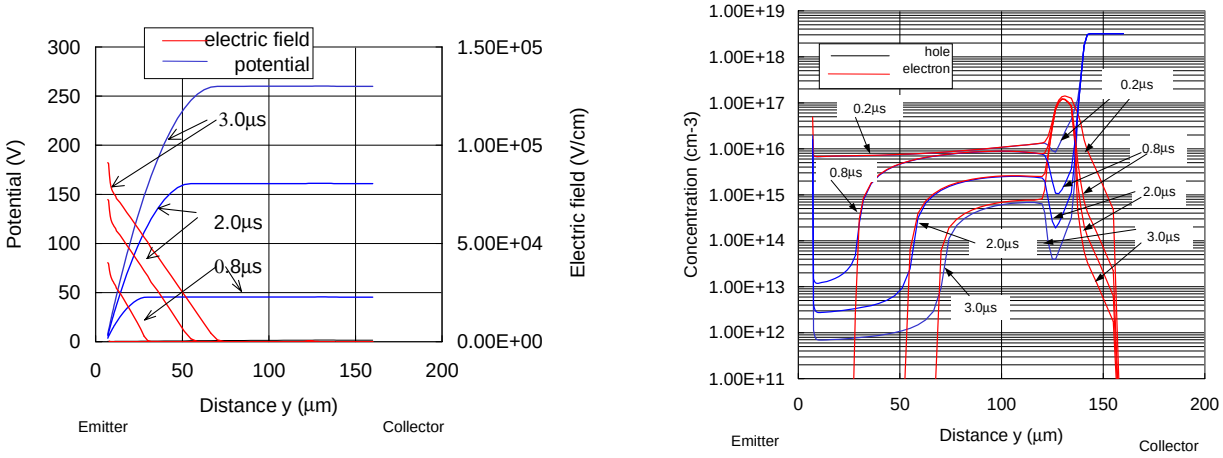


(a) Electric field and potential



(b) Carrier concentration distribution

Fig. 7 Electric field, potential, and carrier concentration distribution of type A under soft switching (dv/dt=100V/μs, other conditions are same as those of Fig. 3.)



(a) Electric field and potential

(b) Carrier concentration distribution

Fig.8 Electric field, potential, and carrier concentration distributions of type B under soft switching (The same conditions as Fig. 7.)